ACD – FORMULARIO

**ANALOG STAGE DESIGN**

MOSFET PARAMETERS

*Ohmic Current:*

*Saturation Current:*

*Overdrive Voltage:*

*Gate Capacitance:*

*Small Signal Parameters:*

*Source Resistance:*

*Drain Resistance:*

*Moderate/Weak Inversion:*

|  |  |  |
| --- | --- | --- |
| *Taxonomy* | *IC values* | *Bias range* |
| *Weak inversion* |  |  |
| *Moderate inversion* |  |  |
| *Strong inversion* |  |  |

*Cut-off Frequency:*

NOISE SOURCES

*Resistor:*

*Mosfet: where in ohmic, in saturation (2 for short ch)*

MOSFET BASIC CONFIGURATIONS

*Common Source:*

*Source Degenerated:*

*Source Follower: if , else*

PROTOTYPICAL DIFFERENTIAL STAGE

*With Resistive Load*

*Differential Mode:*

*Common Mode:*

*With Active (Mirror) Load*

*Differential Mode:*

*Common Mode:*

*White Noise:*

*1/f noise:*

*Corner frequency:*

*Gain Bandwidth Product:*

TWO STAGE OTA

*Differential Gain:*

*Compensations*

*Miller Capacitance:*

# to have stability both the second pole and the positive zero should be moved away from the GBWP, so increasing and reducing the GBWP and the zero that follows it (at least a decade below ), or increasing the transconductance of the second stage, to move the zero away from the GBWP together with the second pole.

*Nulling Resistor:*

# if we set the zero is pushed to infinite. Better if we set so that the zero becomes even negative, best solution put to have a cancellation in phase (-90+90). Starting setting to have , then to have the pole-zero compensation. To build for pole-zero compensation with a transistor with and we need to derive from , and if we have .

*Ahuja Compensation: (if we use a voltage buffer)*

# for values larger than the load capacitance, the second pole is set by , which is usually much smaller than and . Therefore, the ratio needed to reach a given phase margin can be much lower than the value required in the nulling resistor case, thus leading to lower current consumption.

# Finite buffer resistance introduces a left zero and a new HF pole that can become conjugated with the second pole: (if we use a voltage buffer). In the case of Ahuja we can estimate pole positions from expression . Deriving and . This couple of poles degrade the PM of about , being .

*Cascode Compensation: it has the same poles of Ahuja compensation (being , and it has two opposite zeroes at the same frequency: if not used in Cascoded Mirror compensation.*

*Slew-Rate:*

# when we have a two stage amplifier, on the positive slope of the output the limit is set by , on the negative one is the minimum between and .

SINGLE STAGE AMPLIFIERS

*Telescopic cascode amplifier:*

*Folded cascode amplifier:*

CMRR AND OFFSET

*Deterministic Error:*

*Statistical Error:*

*=*

# Many times can be neglected, and also the term if we don’t have a tail generator.

*Voltage Offset:*

*Pelgrom relationship:*

OUTPUT STAGES

**FILTERS DESIGN**

*Selectivity Index:*

*Maximum in-band attenuation:*

*Minimum stop-band attenuation:*

*Discrimination Index:*

*Discrimination Factor:*

BUTTERWORTH FILTERS

*Butterworth Polynomials normalized:*

|  |  |
| --- | --- |
| *N* |  |
| *1* |  |
| *2* |  |
| *3* |  |
| *4* |  |
| *5* |  |
| *6* |  |

*To derive Q:*

*To derive the order n:*

*To derive the cut-off frequency: (where and normalized as well)*

# Starting from the normalized polynomial, once the mask has been remapped (for LP , for HP , for BP where and ), you have to transform it with for LP, for HP, for BP (match the lower limit of the normalized cut-off frequency) and then with for LP, for HP, for BP (shift the cut-off frequency to the desired one).

CHEBYSHEV FILTERS

*Type-1 filters: where are the Chebyshev polynomials and is a coefficient to*

*have for odd n values or for even values of n*

*To derive the order n:*

*To derive the position of the poles:*

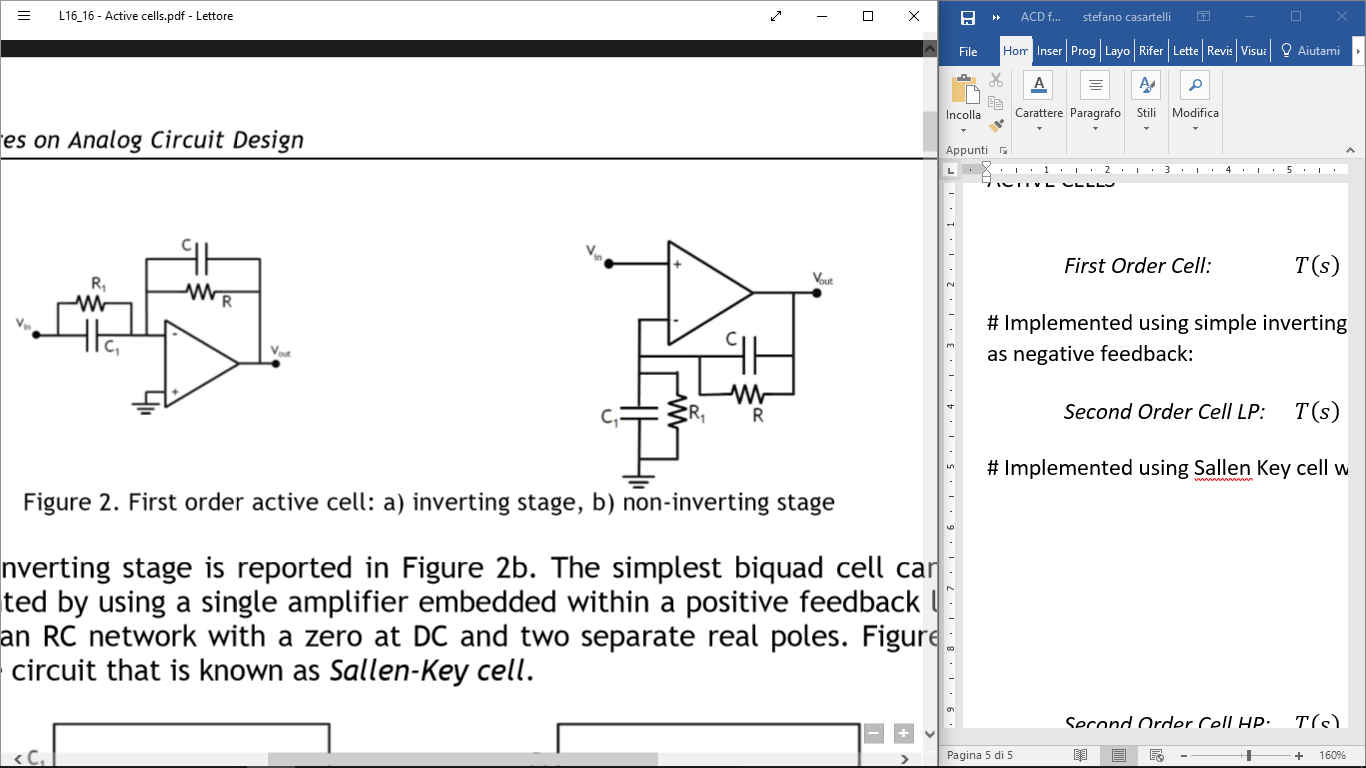
*where*

# Derive the poles and equate the polynomial to the value needed depending on the order to find (write the polynomial as ). Then transform it with for LP, for HP, for BP (shift the cut-off frequency to the desired one).

*Type-2 filters:*

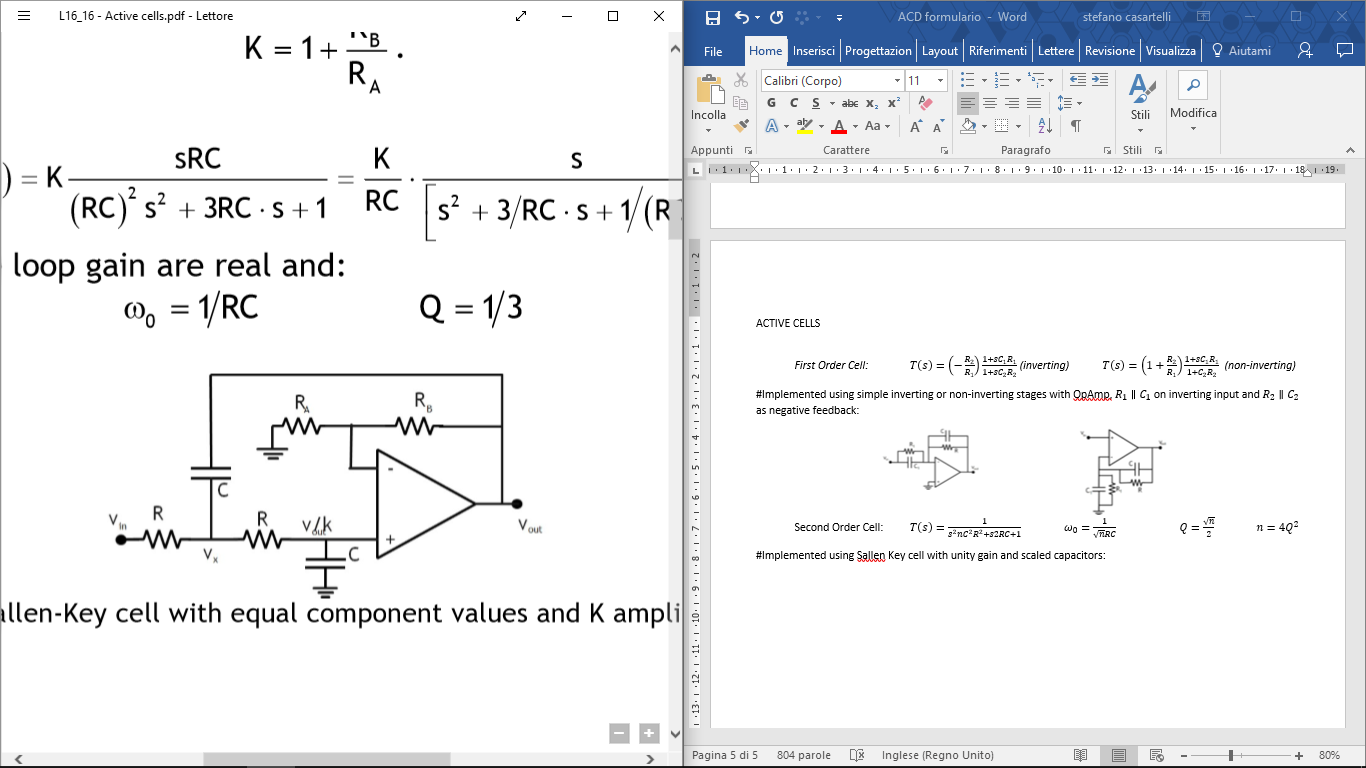
ELLIPTICAL FILTERS

ACTIVE CELLS

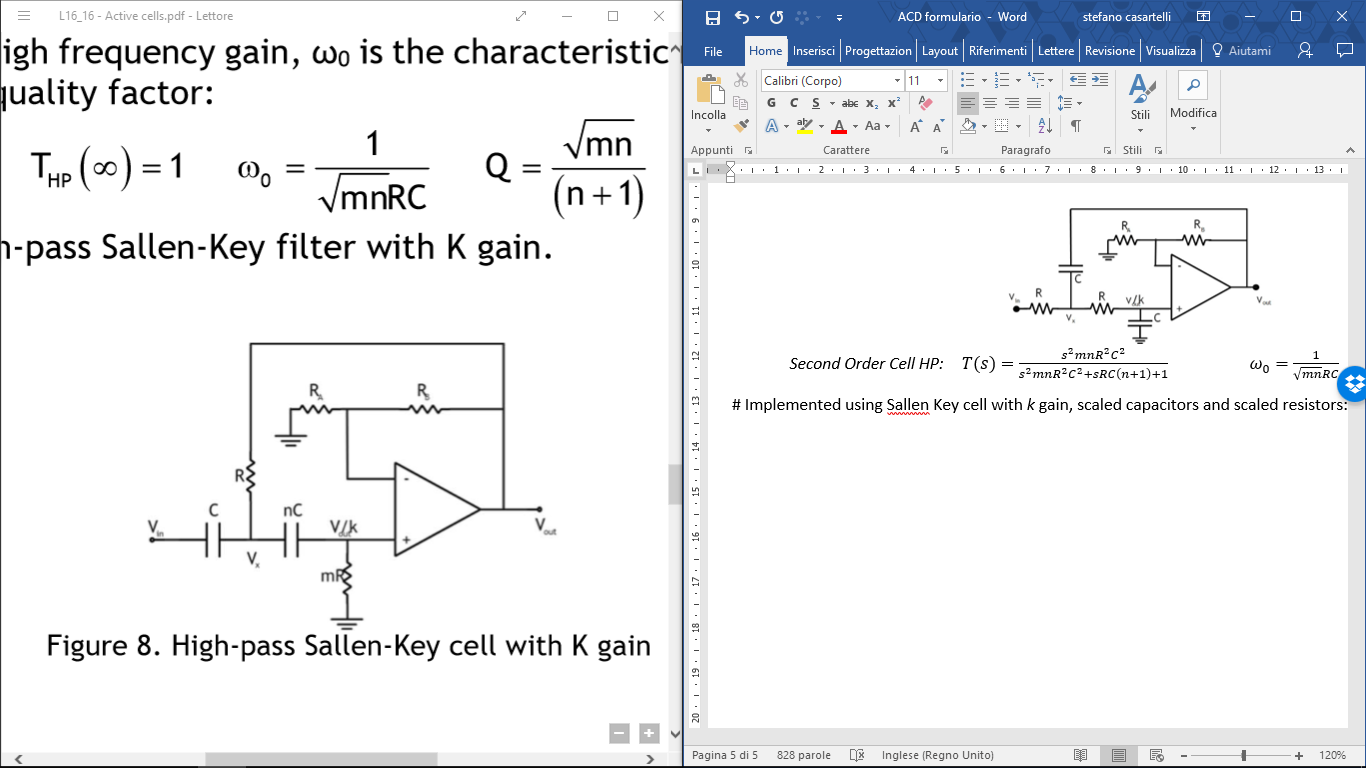
*First Order Cell: (inverting) (non-inverting)*

# Implemented using simple inverting or non-inverting stages with OpAmp, on inverting input and as negative feedback:

*Second Order Cell LP:*

# Implemented using Sallen Key cell with *k* gain and scaled capacitors:

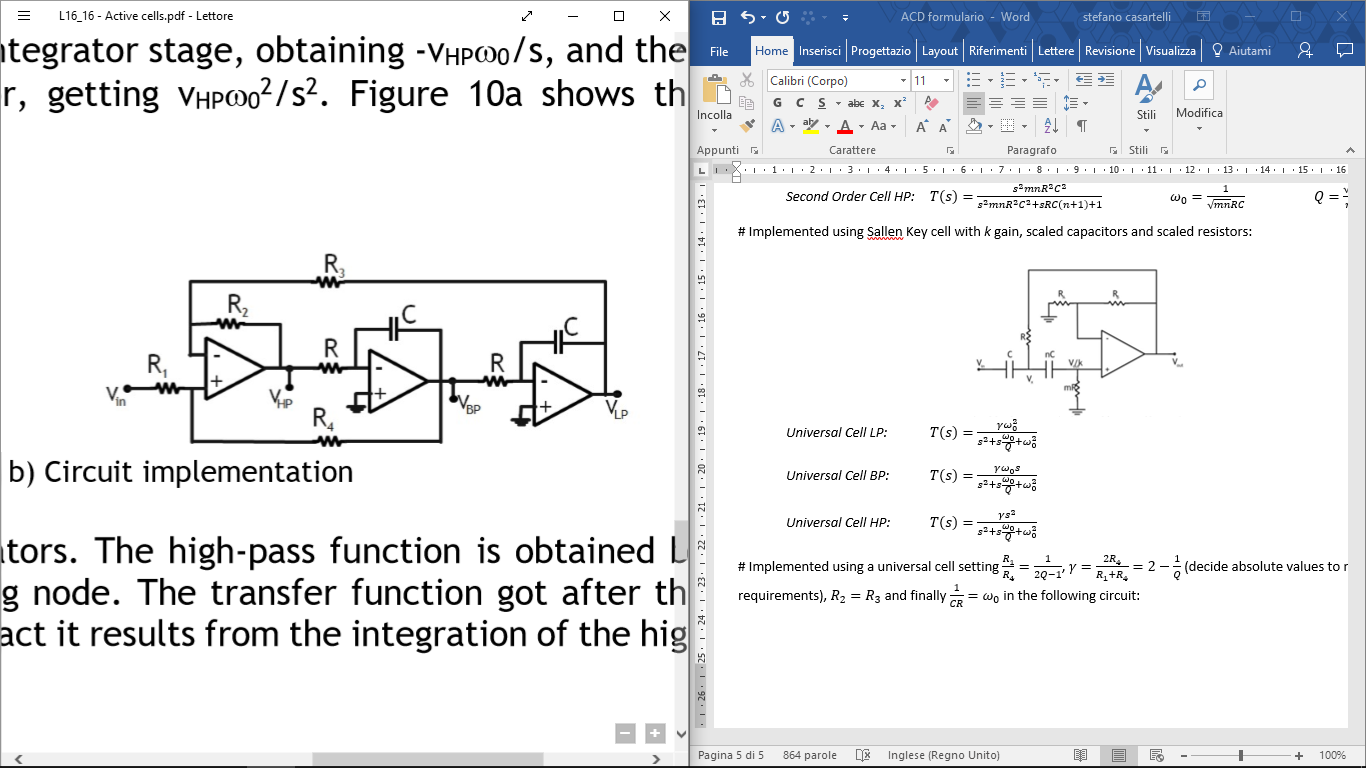
*Second Order Cell HP:*

**# Implemented using Sallen Key cell with *k* gain, scaled capacitors and scaled resistors:

*Universal Cell LP:*

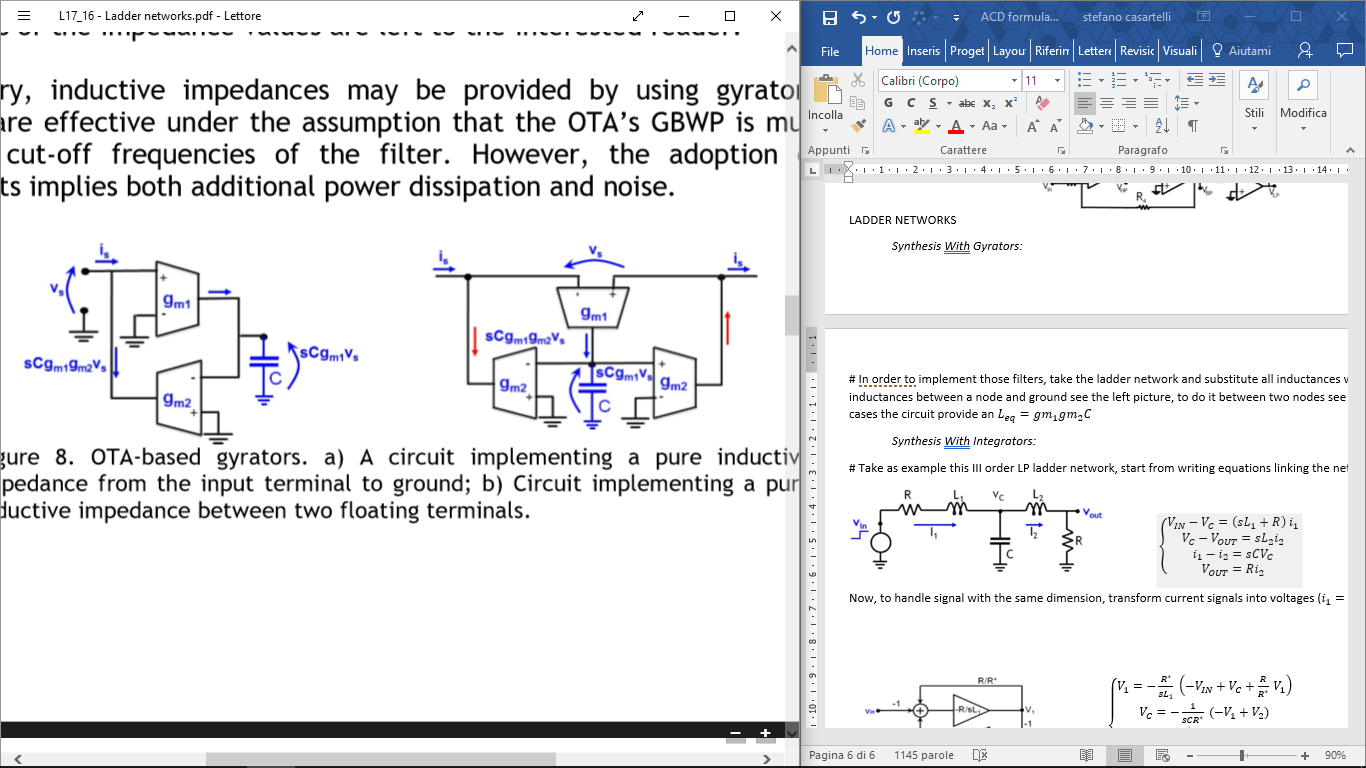
*Universal Cell BP:*

*Universal Cell HP:*

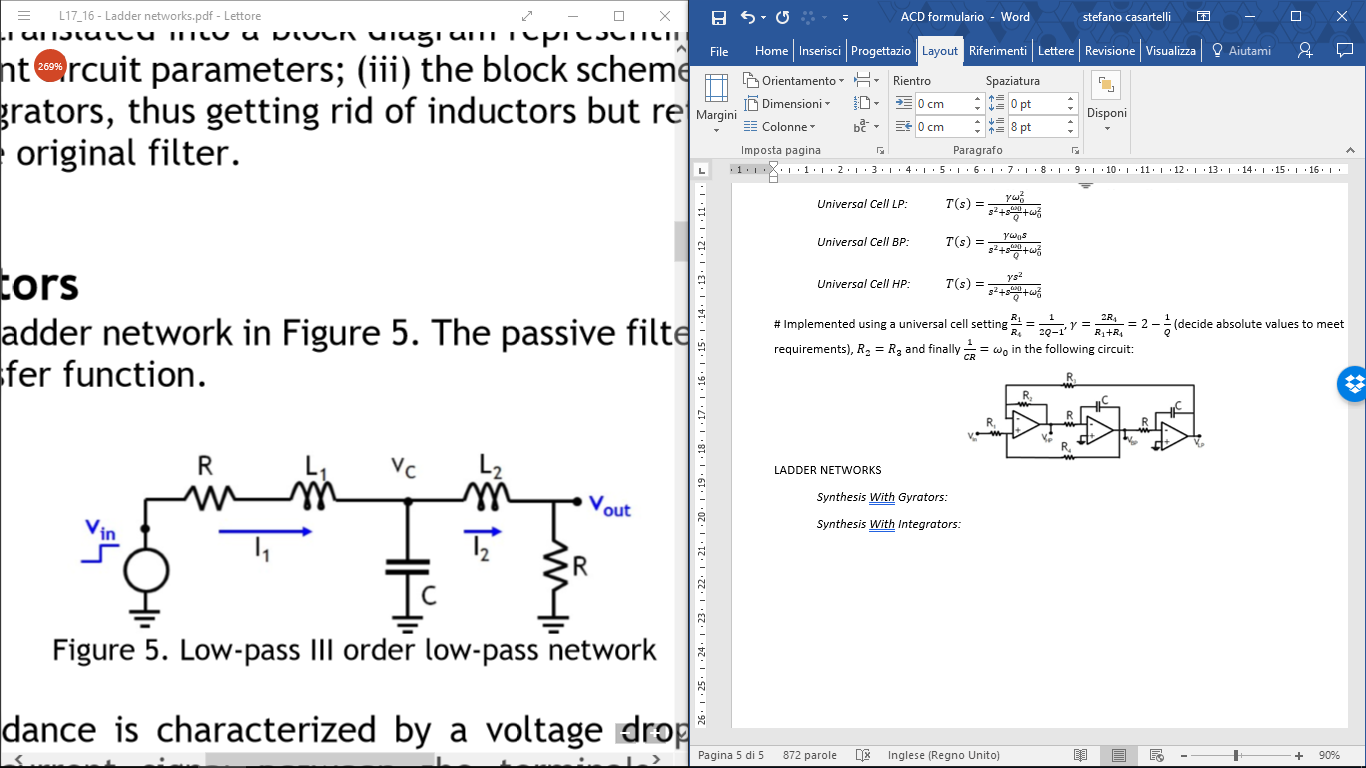
# Implemented using a universal cell setting , (decide absolute values to meet noise requirements), and finally in the following circuit:

LADDER NETWORKS

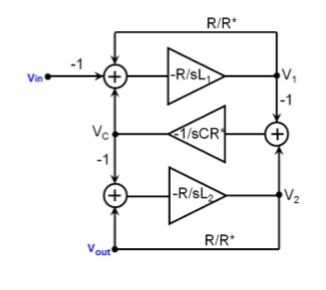
*Synthesis With Gyrators:*

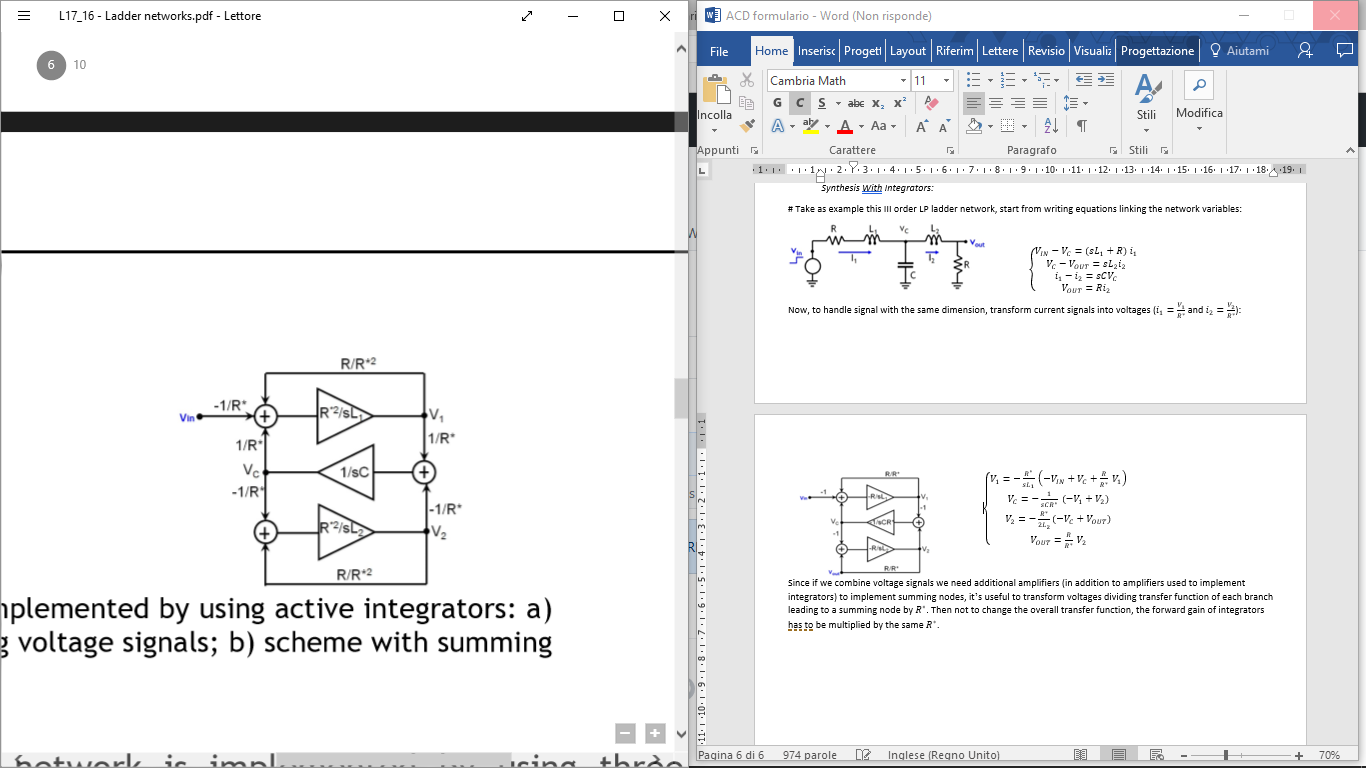
# To implement those filters, take the ladder network and substitute all inductances with gyrators: to create inductances between a node and ground see the left picture, to do it between two nodes see the right one. In both cases the circuit provide an

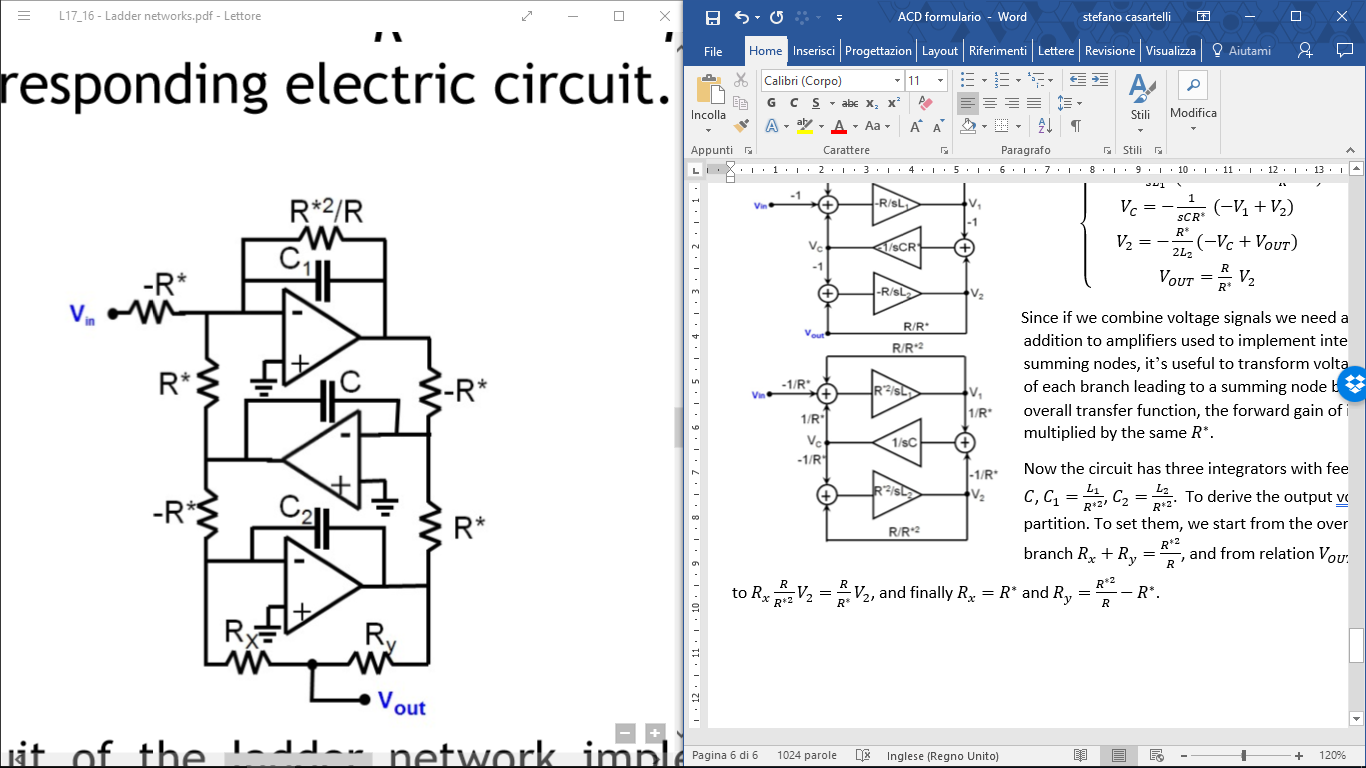
*Synthesis With Integrators:*

**# Take as example this III order LP ladder network, start from writing equations linking the network variables:

Now, to handle signal with the same dimension, transform current signals into voltages ( and ):



Since if we combine voltage signals we need additional amplifiers (in addition to amplifiers used to implement integrators) to implement summing nodes, it’s useful to transform voltages dividing by transfer function of each branch leading to a summing node. Then not to change the overall transfer function, the forward gain of integrators must be multiplied by the same .

Now the circuit has three integrators with feedback capacitances given by , , . To derive the output voltage we need a resistive partition. To set them, we start from the overall resistance along that branch , and from relation , leading to , and finally and .

Obviously we have taken , and to have . We have to resize all these values to match the requested :

Where and is chosen along with to achieve acceptable values for involved capacitances ( some pf).